Transitioning from MLC to TLC flash memory on Raspberry Pi Compute Modules

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Document version history

Release	Date	Description
1	08 Jun 2026	Initial release

Scope of document

This document applies to the following Raspberry Pi products:

Compute Modules

CM0	CM1	CM3	CM3+	CM4	CM4S	CM5
			✓	✓	✓	✓

Introduction

Flash memory (or eMMC) forms the backbone of modern data storage. On Raspberry Pi Compute Modules (not including Lite models), eMMC flash memory is used for program and data storage, as opposed to the SD cards used by our single-board computer range (up to and including Raspberry Pi 5).

At its core, flash memory stores data inside microscopic components called memory cells. The structural differences in how these cells manage electrical charges dictate a drive's speed, reliability, and manufacturing cost.

The two most prominent types of flash memory currently used in computing are **multi-level cell (MLC)** and **triple-level cell (TLC)**. While their names sound similar, their internal architectures and operational characteristics differ significantly.

To date, Raspberry Pi Ltd has used MLC flash memory on all models in the Raspberry Pi Compute Module range. However, in order to secure supply chains and pricing against changes in the eMMC memory market, we have been qualifying various TLC devices for use on our Compute Modules.

Comparing MLC and TLC flash memory

All programmed NAND flash contains bit errors, even within perfect blocks. The bit error rate (BER) is also affected by temperature, and this effect increases as the flash ages.

The fundamental difference between MLC and TLC lies entirely in data density. Data density refers to the number of bits stored inside a single physical memory cell.

Multi-level cell

- **Bits per cell:** Stores exactly **two bits** of data per memory cell
- **Voltage states:** Requires **four distinct voltage levels** (2^2) to represent the binary combinations (00, 01, 10, 11)
- **Performance:** Offers faster write speeds, as the memory controller only needs to target and verify four voltage zones
- **Durability:** Typically endures **3000–10,000 program/erase (P/E) cycles**

Triple-level cell

- **Bits per cell:** Stores **three bits** of data per memory cell
- **Voltage states:** Requires **eight distinct voltage levels** (2^3) to represent combinations from 000 to 111
- **Performance:** Slower native write speeds; program times are longer because bits are programmed in phases across an entire page, with the stored charge decreasing by 1/2, 1/4, and 1/8 of the full-scale voltage
- **Durability:** Typically endures **1000–3000 P/E cycles**

The narrower decoding thresholds for TLC cause the raw bit error rate (BER) to be higher than that of MLC.

Cost versus longevity

TLC provides 50% more storage capacity than MLC using the same number of physical transistors. This higher density makes TLC significantly cheaper to manufacture per gigabyte. However, because the voltage gaps between states are much smaller in TLC, minor electrical leaks caused by physical wear can corrupt data. Therefore, although TLC is much more cost-effective for mass production, MLC is inherently more durable.

NAND cell degradation (in both TLC and MLC) is a function of the number of erase operations on a block. The effects of degradation include a shift in the programmed threshold voltages and an increase in floating gate leakage. As TLC has more voltage levels, this results in lower endurance.

Erase cycle degradation

Erase cycle degradation refers to the physical and electrical wear that flash memory cells experience during program/erase cycles. It primarily stems from the high voltages required to move electrons across a thin insulating oxide layer, which physically damages the material over time.

Both MLC and TLC memory suffer from this degradation. The consequence is that the memory gradually loses its ability to safely store data without power, resulting in increased bit errors and slower P/E speeds. To mitigate these physical limits, modern devices rely on flash controllers equipped with sophisticated algorithms to ensure reliable performance across the rated endurance of the storage media.

The following sections describe these mitigations in more detail, focusing on their use for TLC memory.

Software and firmware adaptations

To make TLC useful for everyday operation despite its lower hardware endurance, manufacturers have had to implement sophisticated software and firmware changes. This typically involves algorithms that run directly on the solid-state drive (SSD) controller inside the eMMC device itself. This has no impact on Compute Module firmware.

Advanced error correction codes (ECCs)

TLC has eight voltage states, meaning electrical noise or cell degradation can result in more frequent data corruption than in MLC.

- **Software change:** Older MLC drives rely on Bose–Chaudhuri–Hocquenghem (BCH) codes for error correction. TLC drives require **low-density parity-check (LDPC)** codes.
- **How it works:** LDPC uses soft-decision decoding — it reads the memory cell multiple times to estimate the probability of a bit being a 1 or a 0. This drastically reduces read errors and artificially extends the lifespan of TLC cells to meet traditional MLC standards.

> **Tip**
>
> In modern flash memory, ECC may use both schemes.

In summary, LDPC codes provide superior robustness in error correction but require parallelised, iterative, soft-decision hardware. Conversely, BCH codes offer lower, deterministic complexity for short-to-medium block lengths. As a result, TLC, which requires the more complex LDPC algorithm, can be slower to read.

Dynamic single-level cell (SLC) caching

The native write speed of TLC is relatively slow due to the precise voltage management required for eight states.

- **Flash controller firmware change:** TLC manufacturers developed **SLC caching**.
- **How it works:** The controller treats a portion of the TLC space as single-level cell memory, writing only one bit per cell instead of three. This enables ultra-fast data transfer during short bursts. When the drive is idle, the controller processes this data in the background, moving it from the fast SLC cache into the denser TLC blocks.

Wear levelling

Allowing a drive to erase the same physical blocks repeatedly will quickly destroy those cells.

- **Flash controller firmware change:** Highly sophisticated **dynamic and static wear levelling** algorithms are integrated into TLC firmware.
- **How it works:** The software tracks the program/erase cycle count of each block on the drive. Dynamic wear levelling rotates newly written data among the empty blocks, while static wear levelling moves rarely modified (‘cold’) data to ensure all of the blocks wear equally. A combination of the two ensures that the entire device wears down at a uniform rate.

Increased over-provisioning management

As flash cells fail, the drive needs spare capacity to replace them without losing user space.

- **Software change:** Flash translation layer (FTL) software reserves a larger percentage of the drive's total raw capacity as hidden space; this is known as **over-provisioning**.
- **How it works:** While an MLC drive might only reserve 7% of its flash blocks for maintenance, a TLC drive often requires 10–15% or more. The firmware uses this space for garbage collection, temporary caching, and replacing worn-out blocks, preventing drive failure. Most eMMC vendors have standardised on 91% user-area availability. Any increase in spare blocks required by TLC is not at the expense of a reduction in free sectors.

Architectural comparison

Table 1.
Architectural comparison

Feature	MLC flash memory	TLC flash memory
Bits per cell	2	3
Voltage states	4	8
Manufacturing cost	Higher	Lower
Data density	Moderate	High
Native lifespan	3000–10,000 P/E cycles	1000–3000 P/E cycles
Primary ECC used	BCH or basic LDPC	Advanced LDPC (soft-decision)

Conclusion

This white paper has described the differences between MLC and TLC flash memory. While TLC has lower cell-level endurance than MLC, its increased capacity and dedicated firmware ensure it is equally reliable.

Raspberry Pi has recently qualified TLC parts for use on Raspberry Pi Compute Modules, and we are confident that they provide comparable performance and endurance.

Contact us for more information

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